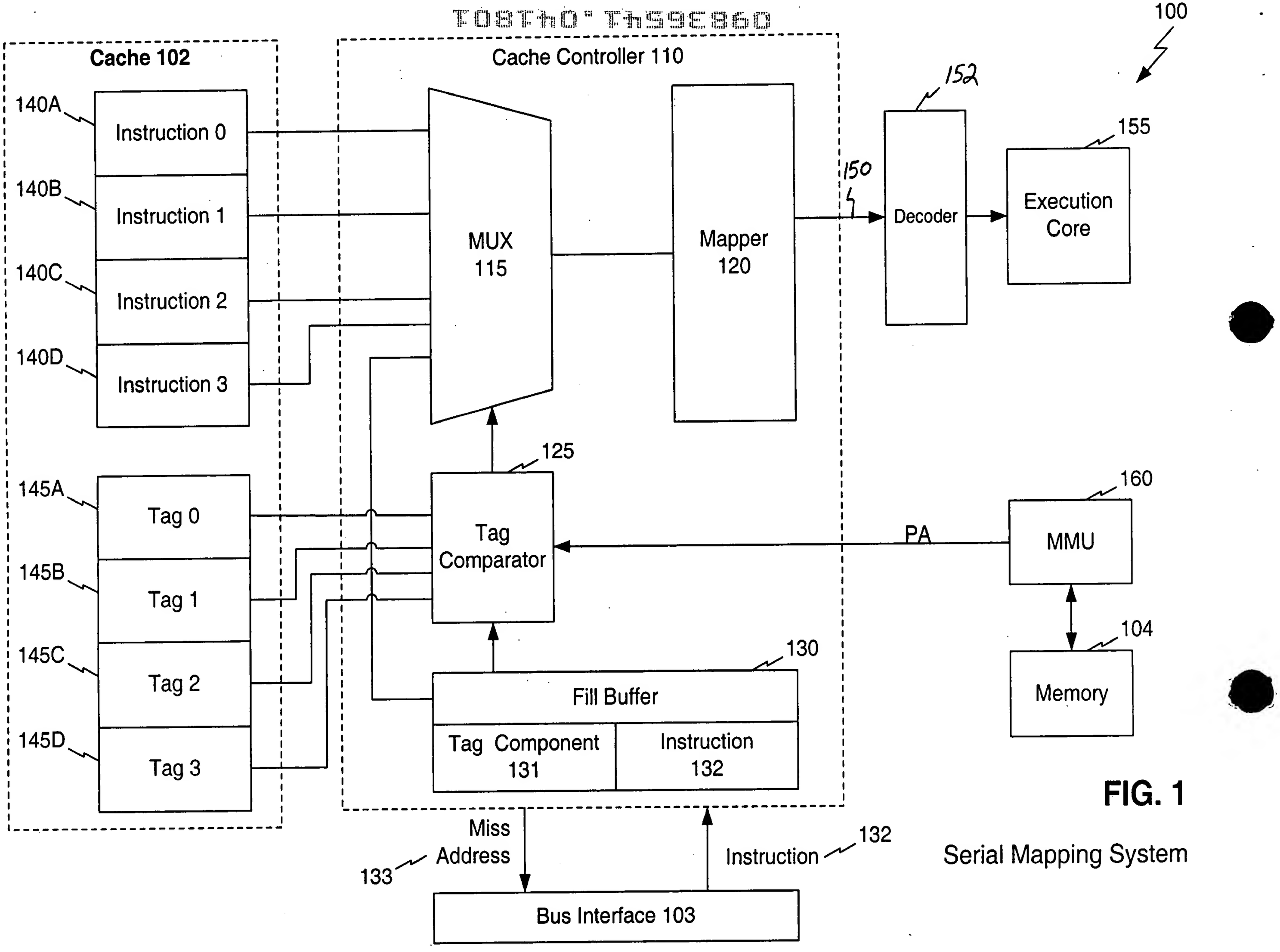

FIG. 1

Serial Mapping System

0101-94.vsd/1

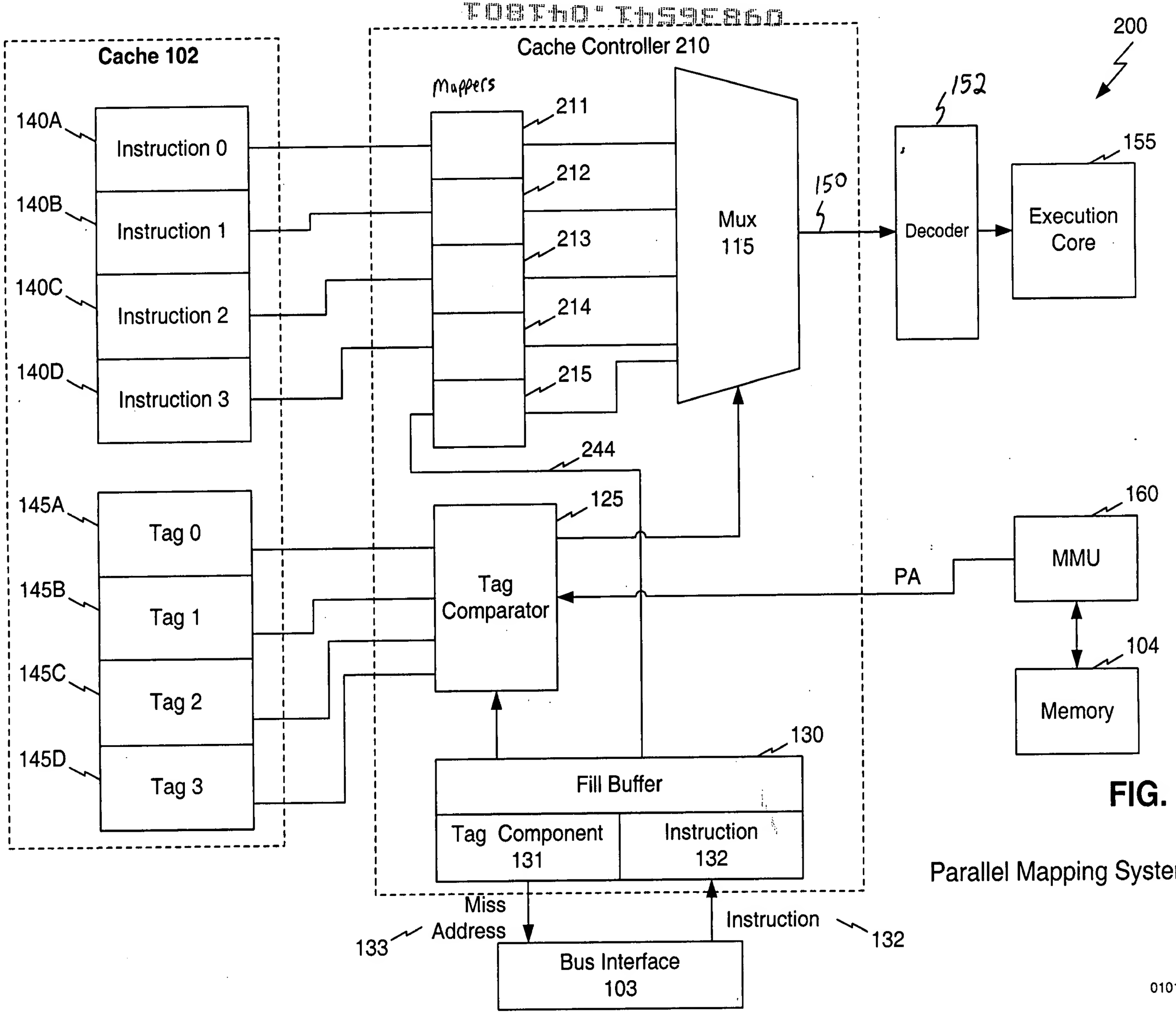

FIG. 2

Parallel Mapping System

0101-94.vsd/2

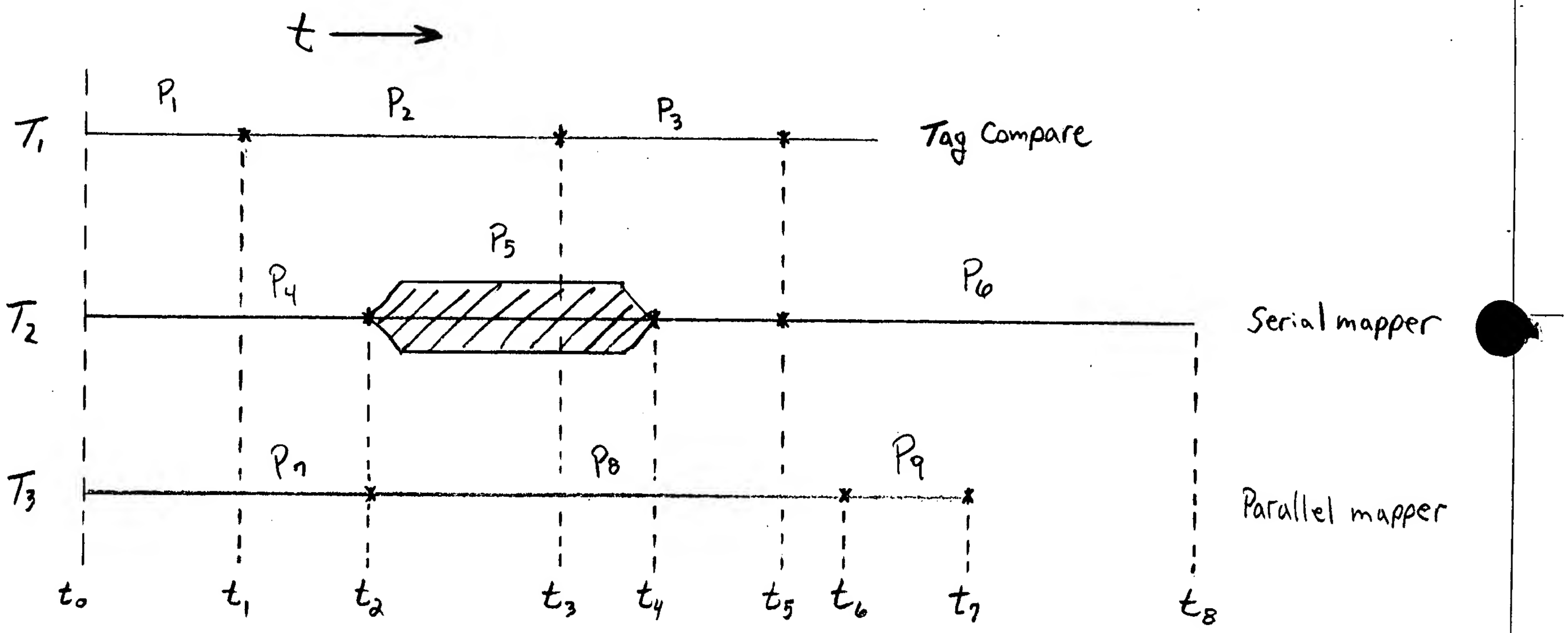

FIG. 3

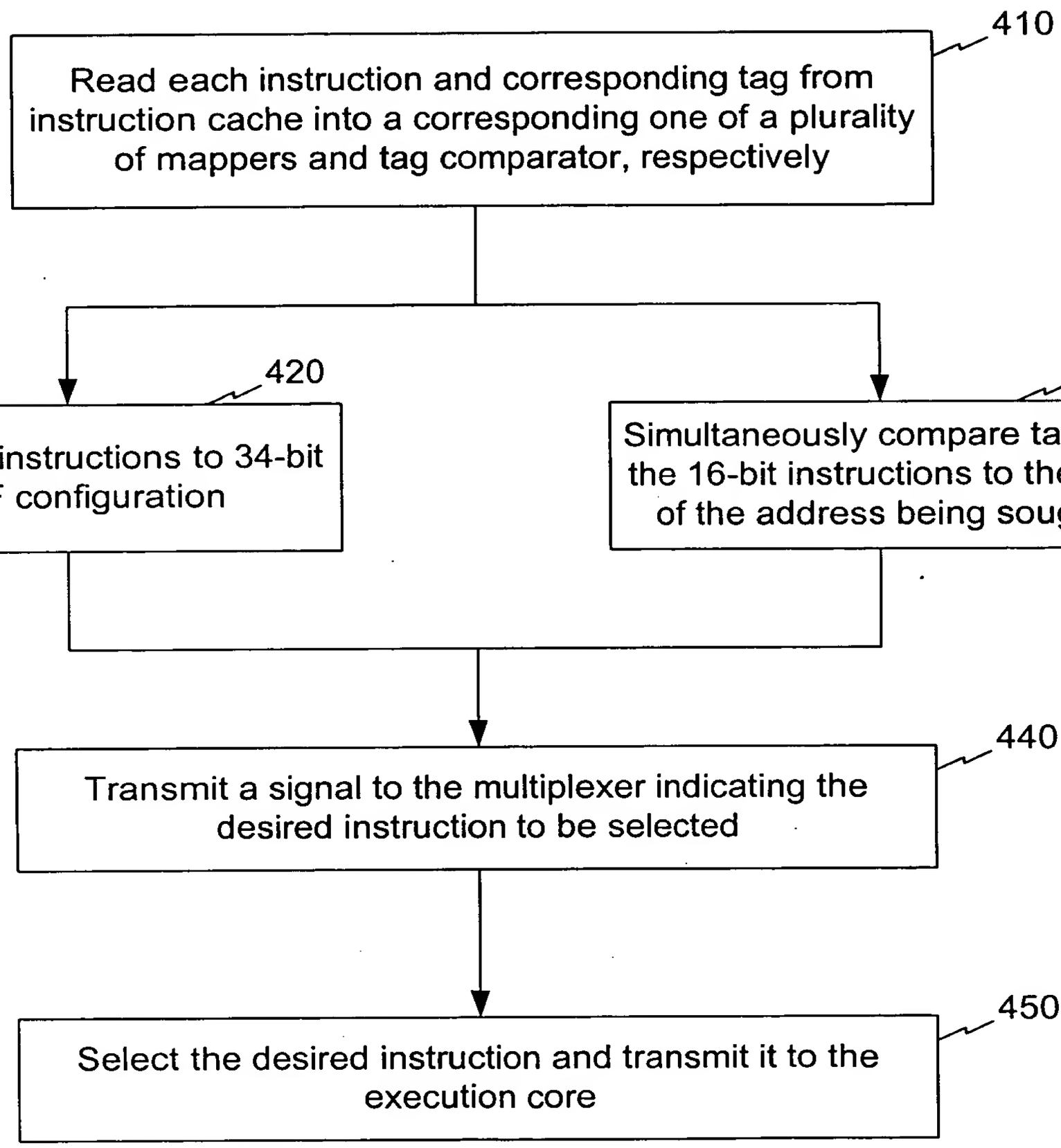
410
Read each instruction and corresponding tag from instruction cache into a corresponding one of a plurality of mappers and tag comparator, respectively
420
Map 16-bit instructions to 34-bit PIWF configuration
430
Simultaneously compare tags of the 16-bit instructions to the tag of the address being sought
440
Transmit a signal to the multiplexer indicating the desired instruction to be selected
450
Select the desired instruction and transmit it to the execution core

FIG. 4

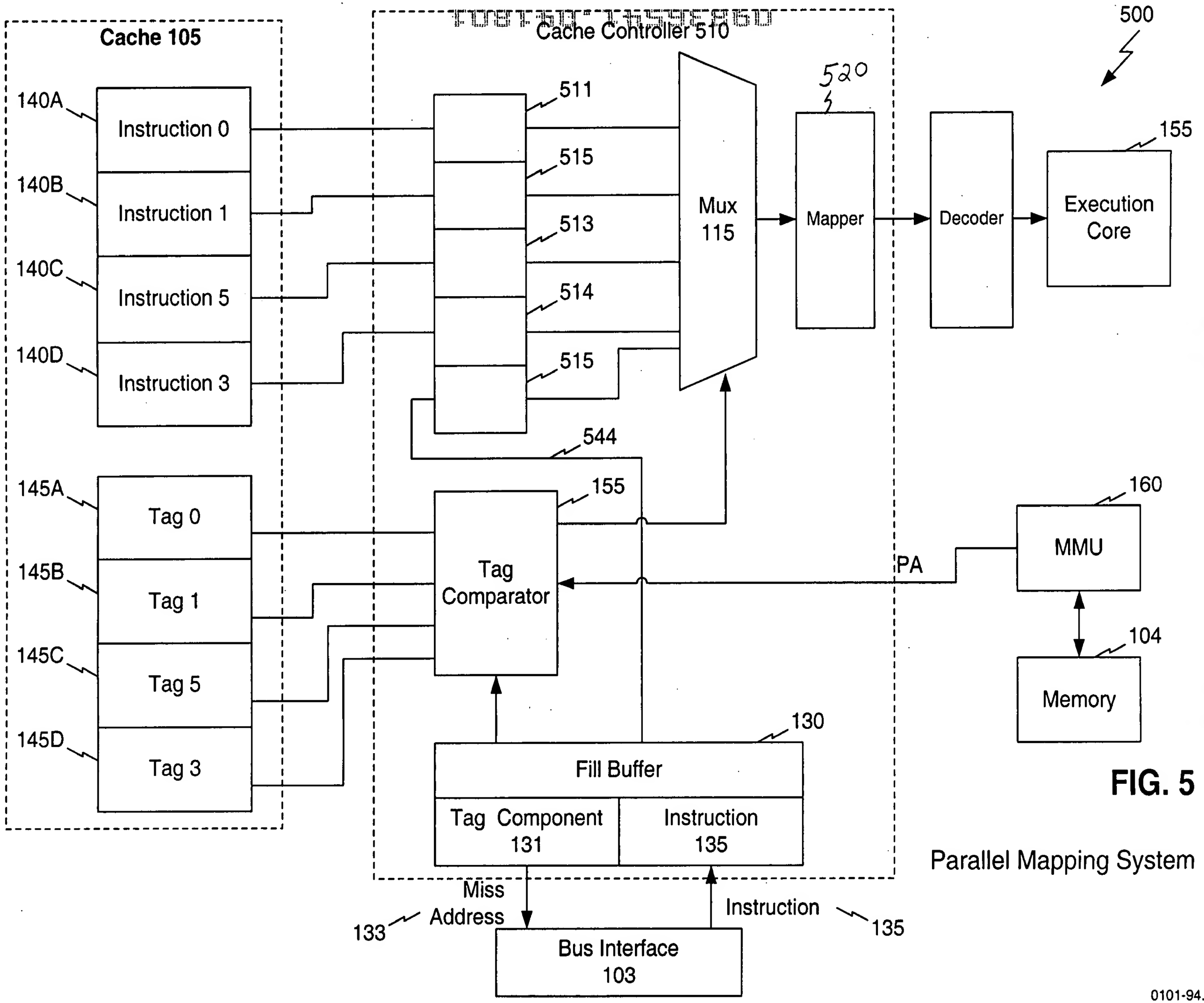

FIG. 5

Parallel Mapping System

0101-94.vsd/5